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|---|---|
| SCHELL, JOSEPH O. | |

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| 2114 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/660,273 | DUNSTAN ET AL. | |
| | Examiner | Art Unit | |
| | Joseph Schell | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13,15-30,32-38 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,15,30,32,33,38 and 40* is/are allowed.

6)☒ Claim(s) *1-12,16-29 and 34-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## *Detailed Action*

Claims 1-13, 15-30, 32-38 and 40 have been examined.

Claims 1-12, 16-29, and 34-37 have been rejected.

Claims 13, 15, 30, 32-33, 38 and 40 are allowed.

### *Response to Arguments*

1. Applicant's arguments filed September 5, 2006 have been fully considered and are persuasive for claims 13, 30 and 38. The arguments regarding claims 1, 16 and 34 are moot in view of the new grounds of rejection.

### *Specification*

2. The disclosure is objected to because of the following informalities:

Page 14, line 14 has a merging of the words "re-availability respectively"

Appropriate correction is required.

### *Claim Objections*

3. Claim 13 lines 16-18 should read "resulting in the set up immediate wake event ~~to~~ immediately ~~wake~~ waking the apparatus and ~~to cause~~ causing the cold start reset processor to be continued as a resume process, wherein the resume process eventually leads ~~leading~~ the apparatus to start operation in an active state continued ~~continuing~~ from the restored operational state of the apparatus.

4. Claims 30 and 38 are objected to for similar grammatical inconsistencies in the last few lines of each claim.

5. Claim 32 line 3 should read "storage does not comprise ~~of~~ a valid saved..."

### *Allowable Subject Matter*

6. Claims 13, 15, 30, 32-33, 38 and 40 are allowed. The following is a statement of reasons for the indication of allowable subject matter: Within independent claims 13, 30 and 38 the examiner deems the novel subject matter to be, within the entirety of each claim, the BIOS as part of the reset process, re-marking a found saved operational state in persistent storage as invalid.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 5-10, 12, 16-17, 20-25, 27, 29, 34-~~36~~ 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson (US Patent Application Publication 2002/0073358) in view of Matsushima ('120).

8. As per claim 1, Atkinson ('358) discloses in an apparatus, a method of operation comprising:

a basic input/output system (BIOS) intervening in a suspend process initiated in response to an AC failure condition of the apparatus (first half of paragraph 40), to place the apparatus in a suspended to memory state (paragraph 40), sustained by backup power (paragraph 40, a low-power mode means that power is consumed more slowly. The examiner is interpreting "sustained by backup power" to mean sustained by this low-power mode. As a backup power supply is not explicitly stated, the broadest reasonable interpretation of "backup power" includes this low consumption mode);

the BIOS initiating as part of the intervention, a plurality of data transfer operations to transfer at least selected contents in a memory of the apparatus to a persistent store to save a persistent copy of an operational state of the apparatus (paragraph 40, the BIOS saves context information and system memory data); and

the BIOS further causing as part of the intervention, at least a processor of the apparatus to operate in a reduced power consumption mode in at least one time period while the BIOS is not performing said checking (paragraph 40, second half, after this backup occurs the suspended state is entered).

Atkinson ('358) does not expressly disclose the system wherein the BIOS further checks, as part of the intervention, one or more times to determine whether the data transfer operations are completed.

Matsushima ('120) teaches a system entering a low-power mode wherein the clock frequency is reduced (see abstract). The CPU can still service asynchronous peripheral devices using a handshaking protocol (column 5 lines 20-24 explain the need for the protocol, column 5 lines 25-34 give more details about the protocol). As part of this protocol, the BIOS read data after it has been written (column 5 lines 47-52).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the low-power mode disclosed by Atkinson ('358) such that a confirmation of the data transfer is performed. This modification would have been obvious because it prevents the loss of data and improves the security of the system (Matsushima ('120) column 5 lines 31-34).

9. As per claim 2, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 1, wherein said causing of at least a processor of the apparatus to operate in a reduced power consumption mode for at least one time period while the BIOS is not performing said checking, comprises the BIOS causing a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking (Matsushima ('120) column 7 lines 58-62, multiple sectors are transferred and besides checking after each sector (and before the next sector), the CPU remains halted).

10. As per claim 5, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 2, wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, is performed after the BIOS initiated the data transfer operations (Matsushima ('120) column 7 lines 58-62, multiple sectors are transferred and besides checking after each sector (and before the next sector), the CPU remains halted).

11. As per claim 6, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 2, wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, is performed after the BIOS determined as part of a checking that the data transfer operations are still in progress (Matsushima ('120) column 5 lines 46-51, each sector of data is checked, with processor halting while waiting for the next transfer completion).

12. As per claim 7, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 2, wherein said causing of at least a processor of the apparatus to operate in a reduced power consumption mode for at least one time period while the BIOS is not performing said checking, further comprises the BIOS setting a timer to expire at the end of the first time period to interrupt the processor, causing the processor to exit the reduced power consumption mode of operation (Matsushima ('120) column 12 lines 38-42).

13. As per claim 8, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 1, wherein said checking comprises the BIOS checking a plurality of times to determine whether the data transfer operations are completed (Matsushima ('120) column 12 lines 63-67, multiple sectors are transferred with a handshaking status reading performed by the BIOS for each transfer).

14. As per claim 9, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 1, wherein said causing comprises the BIOS causing at least a processor of the apparatus to operate in a reduced power consumption mode in a plurality of time periods while the BIOS is not performing said checking (Matsushima ('120) column 7 lines 58-62).

15. As per claim 10, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 1, wherein the method further comprises the BIOS marking the persistent copy of the operational state of the apparatus as valid, upon completion of the data transfer operations (Matsushima ('120) column 5 lines 26-43, the status register is marked by the HDD at the end of transactions initiated by the BIOS).

16. As per claim 12, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 1, wherein the method further comprises the BIOS causing the suspend process to be completed subsequent to the completion of the data transfer

operations (as shown by Atkinson ('358) Figure 3, after each page has been saved (step 310) the suspend to RAM state is entered).

17. As per claim 16, this claim recites limitations found in claim 1 and is rejected on the same grounds as claim 1.

18. As per claim 17, this claim recites limitations found in claim 2 and is rejected on the same grounds as claim 2.

19. As per claim 20, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 17, wherein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, after the BIOS initiated the data transfer operations Matsushima ('120) column 7 lines 58-62, multiple sectors are transferred and besides checking after each sector (and before the next sector), the CPU remains halted).

20. As per claim 21, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 17, wherein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, after the BIOS determined as part of a checking that the data transfer operations are still in progress (Matsushima ('120) column 5 lines 46-51, each sector of data is checked, with processor halting while waiting for the next transfer completion).

21. As per claim 22, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 17, wherein the BIOS causes at least the processor to operate in a reduced power consumption mode for at least one time period while the BIOS is not performing said checking, by further setting a timer to expire at the end of the first time period to interrupt the processor, causing the processor to exit the reduced power consumption mode of operation (Matsushima ('120) column 12 lines 38-42).

22. As per claim 23, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 16, wherein the BIOS checks to determine whether the data transfer operations are completed a plurality of times (Matsushima ('120) column 12 lines 63-67, multiple sectors are transferred with a handshaking status reading performed by the BIOS for each transfer).

23. As per claim 24, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 16, wherein the BIOS causes at least a processor of the apparatus to operate in a reduced power consumption mode while the BIOS is not performing said checking, in a plurality of time periods (Matsushima ('120) column 7 lines 58-62, the CPU is halted while each sector is transferring).

24. As per claim 25, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 16, wherein the BIOS further marks the saved copy of the operational

state of the apparatus as valid, upon completion of the data transfer operations (Matsushima ('120) column 5 lines 26-43, the status register is marked by the HDD at the end of transactions initiated by the BIOS).

25. As per claim 27, this claim recites limitations found in claim 12 and is rejected on the same grounds as claim 12.

26. As per claim 29, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 16, wherein the system is a selected one of a set-top box, an entertainment control console, a video recorder, and a video player (Matsushima ('120) Figure 1A, element 19).

27. As per claim 34, this claim recites limitations found in claim 1 and is rejected on the same grounds as claim 1.

28. As per claim 35, this claim recites limitations found in claim 10 and is rejected on the same grounds as claim 10.

29. As per claim 37, this claim recites limitations found in claim 12 and is rejected on the same grounds as claim 12.

30. Claims 11, 26 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson ('358) in view of Matsushima ('120) and in further view of Thomas ('181).

31. As per claim 11, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 1. Atkinson ('358) in view of Matsushima ('120) does not expressly disclose that the method further comprises the BIOS configuring as part of the intervention, one or more wake events as ineligible to wake the apparatus after the apparatus enters the suspended to memory state, leaving AC re-availability as the only wake event eligible to wake the apparatus from the suspended to memory state.

Thomas ('181) discloses an uninterruptible power supply that prevents a system from resuming operation until additional conditions beyond the restoration of power are fulfilled (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the suspend mode disclosed by Atkinson ('358) in view of Matsushima ('120) such that AC re-availability is the only valid restart event because it would prevent possible data loss (Thomas ('181) column 7 lines 18-34).

32. As per claims 26 and 36, these claims recite the same limitations as claim 11 and are rejected on the same grounds as claim 11.

33. Claims 3-4 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson ('358) in view of Matsushima ('120) and in further view of Mustafa (US Patent 6,243,831).

34. As per claim 3, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 2. Atkinson ('358) in view of Matsushima ('120) does not expressly disclose the method wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, comprises the BIOS causing a processor of the apparatus to enter an ACPI C1 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Atkinson ('358) in view of Matsushima ('120) such that it utilizes the ACPI specification. This modification would have been obvious because it provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to put the system into an ACPI S1 state when waiting for HDD IO. This modification would have been obvious because S1 allows the processor to be turned off, while having very little performance degradation upon returning to normal operation (Mustafa ('831) column 5 lines 53-65).

35. As per claim 4, Atkinson ('358) in view of Matsushima ('120) discloses the method of claim 2. Atkinson ('358) in view of Matsushima ('120) does not expressly disclose the method wherein said causing of a processor of the apparatus to be at least halted for a first time period while the BIOS is not performing said checking, comprises the BIOS causing a processor of the apparatus to enter a selected one of an ACPI C2 state and an ACPI C3 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Atkinson ('358) in view of Matsushima ('120) such that it utilizes the ACPI specification. This modification would have been obvious

because it provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to allow the system to select between ACPI C2 and ACPI C3 states when not performing checking. This modification would have been obvious because ACPI C2 provides more power savings than C1, with slight performance degradation upon resuming normal operation (Mustafa ('831) column 5 lines 59-65), while S3 provides even greater power saving with further degraded performance upon resuming normal operation (Mustafa ('831) column 5 line 66 through column 6 line 5). The BIOS has a list of available sleep states (Mustafa ('831) column 6 lines 26-29), and the time that the processor will be in standby mode varies depending on the transaction (Matsushima ('120) column 7 lines 27-30, the expected frequency of interrupts will vary depending on devices being managed and their needs).

36. As per claim 18, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 17. Atkinson ('358) in view of Matsushima ('120) does not explicitly disclose the system wherein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, by causing the processor to enter an ACPI C1 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Atkinson ('358) in view of Matsushima ('120) such that it utilizes the ACPI specification. This modification would have been obvious because it provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to put the system into an ACPI S1 state when waiting for HDD IO. This modification would have been obvious because S1 allows the processor to be turned off, while having very little performance degradation upon returning to normal operation (Mustafa ('831) column 5 lines 53-65).

37. As per claim 19, Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 17. Atkinson ('358) in view of Matsushima ('120) does not explicitly disclose the system herein the BIOS causes the processor to be at least halted for a first time period while the BIOS is not performing said checking, by causing the

processor to enter a selected one of an ACPI C2 state and an ACPI C3 state for the first time period while the BIOS is not performing said checking.

Mustafa ('831) discloses a system utilizing the ACPI specification with the further provision that BIOS saves the system's state to a hard disk on ACPI S1, S2 and S3 states instead of only on ACPI S4 (column 6 lines 40-48 and a succinctly stated in claim 1).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Atkinson ('358) in view of Matsushima ('120) such that it utilizes the ACPI specification. This modification would have been obvious because it provides a protocol for interaction between a computer system's BIOS and the operating system (Mustafa ('831) column 5 lines 47-52), which would allow for more complicated, and customizable, operating system controlled BIOS operations.

It would have additionally been obvious to allow the system to select between ACPI C2 and ACPI C3 states when not performing checking. This modification would have been obvious because ACPI C2 provides more power savings than C1, with slight performance degradation upon resuming normal operation (Mustafa ('831) column 5 lines 59-65), while S3 provides even greater power saving with further degraded performance upon resuming normal operation (Mustafa ('831) column 5 line 66 through column 6 line 5). The BIOS has a list of available sleep states (Mustafa ('831) column 6

lines 26-29), and the time that the processor will be in standby mode varies depending on the transaction (Matsushima ('120) column 7 lines 27-30, the expected frequency of interrupts will vary depending on devices being managed and their needs).

38. Claims 28 and 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson ('358) in view of Matsushima ('120) as applied to claim 16, and in further view of Sadashivaiah (US Patent 5,638,541).

Atkinson ('358) in view of Matsushima ('120) discloses the system of claim 16. Atkinson ('358) in view of Matsushima ('120) does not expressly disclose the system further comprising a networking interface operatively coupled to the BIOS.

Sadashivaiah ('541) teaches a power management driver that intercepts power down requests and reissues them to the BIOS such that it can micromanage which devices are placed in standby mode (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Atkinson ('358) in view of Matsushima ('120) such that it uses a power management driver as a BIOS interface for standby and wakeup events. This modification would have been obvious because it would allow the system to periodically wake and service network queries and maintain a network connection

while otherwise maintaining a standby state (Sadashivaiah ('541) column 5 line 64 through column 6 line 45).

39. As per claim 33, this claims recites limitations found in claim 28 and is rejected on the same grounds as claim 28.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Specifically, Itoh ('675) teaches a system wherein multiple users can maintain individual saved states when power fails.

### *Contact Information*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

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SUPERVISORY PATENT EXAMINER